STABILITY OF AMORPHOUS/CRYSTALLINE SILICON HETEROJUNCTIONS

Ştuart Bowden¹, Ujjwal Das³, Stanislau Herasimenka¹ and Robert Birkmire¹,²
¹Institute of Energy Conversion, University of Delaware, Newark, DE 19716
²Department of Physics and Astronomy, University of Delaware, Newark, DE 19716

ABSTRACT

Silicon heterojunction solar cells have demonstrated high efficiencies through excellent surface passivation. However, the use of amorphous silicon (a-Si) in the structure raises the question of long term stability as a-Si solar cells suffer degradation due to the Staebler-Wronski effect. The stability of a-Si in terms of its ability to passivate silicon wafers is evaluated by measuring the minority carrier lifetime and it is found to be unstable over time. The instability is most evident in thin, ~ 10 nm, intrinsic a-Si only layers where lifetime falls from over 1ms immediately after annealing, to 300 µs one month later. The change in lifetime occurs even in the dark at room temperature with the largest fall in the first few days after deposition. The lifetime can be recovered close to its initial level by annealing the sample in air, indicating that the lifetime change is not due to a simple oxidation of the outer layer of a-Si. However, device measurements where an intrinsic/doped a-Si structure is used for the emitter and contact show no change in open circuit voltage or fill factor after one year. The changes in the passivation during processing has important implications for the sequence of device fabrication, the use of lifetime testing as a diagnostic tool and the passivation of all back contact devices.

INTRODUCTION

Heterojunctions between amorphous silicon (a-Si) and crystalline silicon (c-Si) have demonstrated high efficiencies in excess of 20% in both research and production [1]. The key to the high efficiency is the very high open circuit voltage (Voc) obtained by using an intrinsic a-Si layer to passivate the surfaces of a silicon wafer.

Crystalline and amorphous silicon have both been used extensively by themselves to create homojunction devices. Crystalline silicon cells using diffusion junctions are generally stable, although defects such as boron-oxygen pairs in p-type silicon lead to a 4-7% relative reduction in efficiency in manufactured devices [2]. In contrast, a-Si solar cells have shown poor stability, primarily due to light induced degradation by the Staebler-Wronski effect [3]. Typical single junction a-Si devices decline in efficiency by 20% relative after light soaking for around 100 hours [4]. Process engineering and device design has reduced the impact of the instability present in hydrogenated a-Si devices, but any structure using a-Si raises the question of long term device stability. The intrinsic a-Si layer is the key to the high voltage of the silicon heterojunction solar cell and the deposition conditions are similar to those used in creating an all amorphous p-i-n solar cell. Due to the importance of the intrinsic layer the measurement before the application of the doped layers provides an important diagnostic tool for process optimization. The use of a-Si as a passivation without doped layers is also important for back contact devices.

Despite the extensive interest in silicon heterojunction devices, the stability of the cells and the passivation by the amorphous silicon layer have only been briefly discussed in the literature. Cell stability has only been measured over periods of hours [5][6]. The stability of the amorphous films has only been reported in the context of subsequent processing at high temperature [7][8], exposure of aSi/SiN stacks under UV light[9], or over a limited time period [10].

In this paper, we examine two questions 1) the stability of passivation afforded by layers of a-Si on c-Si and 2) determine the stability of silicon heterojunction solar cells.

SAMPLE PREPARATION

To examine the surface passivation, films of intrinsic a-Si are applied to a silicon wafer. The substrates are double-side polished high-lifetime float-zone with a thickness of 280 µm. The wafer resistivity is nominally 1 Ω cm of both n and p-type. The wafers are cleaned using a piranha etch (H₂SO₄/H₂O₂), followed by a DI water rinse, a dip in dilute HF and immediate transferal to the deposition system. The depositions are performed in a plasma enhanced chemical vapor deposition (PECVD) system at a temperature of 200 °C. The intrinsic films use hydrogen and silane at ratio of 2:1 to ensure amorphous rather than epitaxial growth [11]. The wafer is flipped over within the system so that both sides of the wafer are deposited without breaking vacuum. Following the deposition the wafers are annealed at 300 °C in vacuum. We have found that the anneal works equally well in air.

The minority carrier lifetime is measured using a Sinton WCT-100 and in all cases reported at a minority carrier density of 10¹⁵ cm⁻³. The high lifetime float-zone substrates caused the measured effective lifetime to be dominated by recombination at the a-Si/c-Si interface. The lifetime of the substrates is expected to be stable since all processing is performed below 300 °C and the low oxygen content of FZ eliminates defect pairs [2].
LIFETIME STABILITY

The lifetime as shown in Figure 1 begins to decline immediately after deposition and continues to decline even after six months. The lifetime decline is occurs in all both (100) and (111) wafers. We have found similar lifetime instabilities on all wafers monitored but the lifetime degradation does seem to be greater on higher lifetime material. Hydrogenated a-Si is known to suffer from the Staebler-Wronski effect caused by the recombination of light generated carriers. However, since these samples are stored in the dark the decline appears to be unrelated to the Staebler-Wronski effect. The process of taking the lifetime measurement exposes the wafer to a short pulse of light of high intensity up to 10 suns. However, for the measurements reported in this paper the measurement was done in transient mode with a short flash duration of only ~100 µs. The lifetimes are stable if repeated measurements are taken over a short time period of a few minutes. The lifetimes are also found to be stable if the sample is exposed to repeated flashes with a longer duration of 12 ms, (for quasi-steady-state measurements) and then retested using the 100 µs flash.

A possible mechanism for the lifetime degradation is the oxidation of the outer layer of a-Si as the samples are stored in room air. However, Figure 1 and 2 show that the lifetime can be recovered by further annealing the wafer in air at ~ 300 °C for 20 min. The recovery is repeatable but not completely reversible. Over time the lifetime after annealing also continues to decline.

We have previously found that we get similar lifetime improvements whether we anneal the wafers in either air or vacuum. Since the air anneal should further oxidize the outer layer of a-Si, oxidation is unlikely to be the cause of the decline in lifetime. FTIR measurements indicate a change in the surface of the a-Si rather than the interface and suggest that water adsorption on the surface is a possible cause. Heating the sample is likely to drive off the surface water molecules and return the surface to the original state.

To determine the cause of the lifetime decline, the a-Si layer was capped with SiN to stabilize the surface. Even for very thin a-Si layers of only 5 nm, there is no change in the lifetime after one month with the SiN cap as can be seen in Table I. A substrate with 20 nm of a-Si also shows a drop in lifetime after one month.

Table I: Stability of a-Si silicon layers on n-type crystalline silicon. Capping the layer with SiN prevents the adsorption of moisture at the surface and stabilizes the film.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Initial (µs)</th>
<th>1month (µs)</th>
<th>% fall</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 nm i-layer (polished)</td>
<td>2082</td>
<td>1006</td>
<td>52</td>
</tr>
<tr>
<td>20 nm i-layer (Textured)</td>
<td>367</td>
<td>226</td>
<td>38</td>
</tr>
<tr>
<td>80 nm SiN on 5 nm i-layer</td>
<td>1585</td>
<td>1527</td>
<td>4</td>
</tr>
<tr>
<td>80 nm SiN on 5 nm i-layer (second sample)</td>
<td>1154</td>
<td>1118</td>
<td>3</td>
</tr>
</tbody>
</table>

In the silicon heterojunction structure the thin amorphous layers are covered with doped layers to form a solar cell. In our case, the cells are typically fabricated on an n-type substrate and the front of the solar cell consists of a 10 nm i-layer followed by a 10 nm layer of p-type a-Si. Similarly, the rear surface of the cell consists of a 10 nm i-layer capped by a 30 nm layer of n-type a-Si.

Capping the intrinsic a-Si layer with doped layers for a solar cell stabilizes the surface as shown in Figure 3. It is
interesting to note that the front surface is still quite thin with a total thickness of only 20 nm.

![Figure 3](image-url) Figure 3: The lifetime is stable once the 10 nm i-layers of a-Si have been capped with doped layers as for a solar cell. The two data sets are companion wafers from the same batch. The structure is 10 nm p-type a-Si/10 nm intrinsic a-Si/280 µm 1 ohm cm n-type c-Si/10 nm intrinsic a-Si/30 nm n-type a-Si.

## STABILITY OF COMPLETED SOLAR CELLS

To measure the stability of finished devices a series of cells was measured over a period of over one year. A group of four cells was initially measured to have \(V_{OC}\) of about 680 mV. High voltage cells were chosen as these are the most sensitive to changes in recombination centers. After storage the dark for nine months, the \(V_{OC}\) of the cells was found to have changed by less than 2 mV. The cells were then illuminated for a further period of almost six months as shown in Figure 4. Over this time period the cells were illuminated with around one sun illumination at a temperature of 45–50 °C. The cells were removed from the stability chamber and measured at standard test conditions (AM1.5, 25 °C, 100 mW/cm\(^2\)) using a calibrated light source. After over a year (9 months in the dark and 6 month illumination), the \(V_{OC}\) of the cells has changed by only a few mV, well within the natural drift of the system caused by temperature fluctuation during measurement, indicating that the recombination mechanisms within the device have not changed.

![Figure 4](image-url) Figure 4: \(V_{OC}\) stability of four cells after almost 6 months exposure to 1 sun illumination. The \(V_{OC}\) change is less than 2 mV in all cases. The lines are linear fits to the data.

The efficiency of the four devices is shown in Figure 5 below. The efficiency is largely unchanged with an average change in efficiency over six months of < 0.2 \%. These devices are small area laboratory cells that were not intended for long term testing so the fact that they are stable without encapsulation is remarkable.

![Figure 5](image-url) Figure 5: Efficiency of the four cells of previous figure. The lines are linear fits to the data. The scatter is primarily caused by fill factor variations.

### Stability of Czochralski Substrates

The results reported in the previous sections of the paper are on float-zone (FZ) material. For p-type substrates there is a substantial difference in performance between expensive FZ material and commercial grade
Czochralski (Cz) material [2]. For n-type substrates we have found similar minority carrier lifetimes in FZ and Cz material, with both types measuring in excess of 1 ms. The stability of the n-type material is further confirmed by our devices sent to NREL for independent measurement. An 18.4 % efficient cell tested 692 mV at IEC and 694 mV at NREL six weeks later. Upon return to IEC two months later, the cell still tested 692 mV. While the testing procedure has not been as rigorous as for the FZ cells of Figure 4, there is no evidence that n-type commercial grade Cz wafers exhibit any instability.

CONCLUSION

Thin amorphous silicon layers are shown unstable as exhibited by a fall in minority carrier lifetime over time. The instability is prevented by capping the layer with either a layer of silicon nitride or a layer of doped amorphous silicon. Silicon heterojunction solar cells are stable even with light soaking of almost six months. No instability was shown in either high purity FZ or commercial grade Cz n-type devices.

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REFERENCES